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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,499	01/22/2002	Jin-Yuan Lee	MEGP0012USA	7456

27765 7590 11/30/2007
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
11/30/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
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Office Action Summary	Application No.	Applicant(s)	
	10/055,499	LEE ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *281-370* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *281-370* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 9/13/07.

Claims **281-370** are pending in this application.

Claims **1-280** have been cancelled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 281 and 287-300 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (6,396,148 hereinafter "Eic-148" of record) in view of Kim (6,025,995 of record).

Regarding claims 281, 287-291, 293, 295-298 and 300, "Eic-148" discloses Regarding claims 281, 287, 288, and 291, 294-296, Eichelberger (see specifically figures 1 and 2-4) discloses a method for fabricating a circuit component comprising: joining a plurality of dies (102) having conductive pads (107) on a top surface of a substrate (101) via an adhesive material (103); forming a polymer layer (104/106) over the substrate (101), wherein the polymer layer comprises a first portion (106) over the die (102) and a second portion (104) over the substrate (101) and around the dies (102) but not over the dies (102), and wherein the second portion (104) has a surface coplanar with an active surface of the die (102); curing the polymer layer (106); removing (or etching) portions of the polymer layer (106) to form via holes (122) (See Fig. 3D); texturing (or grinding) the surface of the polymer layer (106) for improving adhesion of the

metallization to the polymer surface (Col. 6, lines 50+); forming a circuit layer (108/109) by electroless plating (Col. 8, lines 27+) over the dies and across an edge of the die (102); forming solder bumps (110) over the circuit layer, wherein at the bump (152/154) can be positioned over the substrate but not over the dies (see figure 1) and comprises solder. "Eic-148" further discloses cutting the substrate (by sawing (Col. 8, lines 47+) being considered as mechanical cutting), after forming the solder bumps (110), the insulating layer (106), the circuit layer (108/109), to obtain individual packaged module as being show in Figure 1 (Col. 8, lines 46+). "Eic-148" fails to teach the bump (110) being a gold bump.

Gold, however, is a known material and commonly used in semiconductor art for forming bumps as disclosed by Kim (Col. 6, lines 59+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to select gold for forming bumps in "Eic-148" chip package since gold bumps is commonly used in semiconductor art, as disclosed by Kim. Motivation to do so would have improved the electrical connection and prevented the oxidization of the bumps.

Regarding claims 292, 294 and 299, although the proposed method of "Eic-148" and Kim lacks an inclusion of the use of sputtering to form the circuit layer, selecting a specific type of known available process (See "Eic-148" Col. 1, lines 46+), in semiconductor art, for forming a circuit layer on the die would have been obvious to one of ordinary skill in the art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify "Eic-148" and Kim accordingly in order to provide a suitable circuit layer for the intended target of the device structure. The selection of electroplating process for forming the circuit layer in claim 292, and laser

cutting process for separating the substrate in claim 299, would have also been obvious for similar reasons set forth above (as evidenced by Konrad, U.S. Patent No. 6,730,857, Col. 4, lines 15+).

3. Claims 282, 301-316, and 318, are rejected under 35 U.S.C. 103(a) as being unpatentable over "Eic-148" (of record) in view of Wojnarowski (5,576,517 of record).

Regarding claims 282, 301, 303, 305, 307, 309-316, and 318, "Eic-148" (see specifically figures 1 and 2-4) discloses a method for fabricating a circuit component comprising: joining a plurality of dies (102) having conductive pads (107) on a top surface of a substrate (101) via an adhesive material (103); forming a polymer layer (104/106) over the substrate (101), wherein the polymer layer comprises a first portion (106) over the die (102) and a second portion (104) over the substrate (101) and around the dies (102) but not over the dies (102), and wherein the second portion (104) has a surface coplanar with an active surface of the die (102); curing the polymer layer (106); removing (or etching) portions of the polymer layer (106) to form via holes (122) (See Fig. 3D); texturing (or grinding) the surface of the polymer layer (106) for improving adhesion of the metallization to the polymer surface (Col. 6, lines 50+); forming a circuit layer (108/109) by electroless plating (Col. 8, lines 27+) over the dies and across an edge of the die (102); forming solder bumps (110) over the circuit layer, wherein at the bump (152/154) can be positioned over the substrate but not over the dies (see figure 1) and comprises solder. "Eic-148" further discloses cutting the substrate (by sawing (Col. 8, lines 47+) being considered as mechanical cutting), after forming the solder bumps (110), the insulating layer (106), the circuit layer (108/109), to obtain individual packaged module as being show in Figure 1 (Col. 8, lines 46+). "Eic-148" does not specifying the insulating layer comprising a porous structure.

Wojnarowski et al. while related to a similar structure design teach (see specifically figures 1-11) teach an insulating layer (20) comprising a porous structure being deposited over the die (14) (Col. 5, lines 9+), which is mounted on the substrate (10). The purpose of using the insulating layer comprised a porous structure is to reduce the dielectric constant of the insulating layer (as close to 1 as possible and not greater than about 2, Col. 3, lines30+) so that it can reduce the need for laser ablation of material situated over air bridge structures and other microwave structures and devices (Col. 3, lines 45+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that applying the low dielectric constant porous layer, as taught by Wojnarowski, to "Eic-148" method would have been beneficial because it helps to provide a low dielectric constant insulating layer which can apply to form high frequency circuits and reduce the need for laser ablation of material situated over air bridge structures and other microwave structures and devices.

Regarding claims 302, 304, 306, and 308, although the proposed method of "Eic-148" and Wojnarowski lacks an inclusion of the use of sputtering to form the circuit layer, selecting a specific type of known available process (See "Eic-148" Col. 1, lines 46+), in semiconductor art, for forming a circuit layer on the die would have been obvious to one of ordinary skill in the art. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify "Eic-148" and Wojnarowski accordingly in order to provide a suitable circuit layer for the intended target of the device structure. The selection of electroplating process for forming the

circuit layer in claims 302 and 306, would have also been obvious for similar reasons set forth above (as evidenced by Konrad, U.S. Patent No. 6,730,857, Col. 4, lines 15+).

4. Claims 283-286 and 320-370 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Eic-148" of record in view of Kim (6,025,995 of record) and further in view of Saia (5,874,770 of record).

Regarding claims 283-286 and 320-370, the proposed method of "Eic-148" and Kim discloses all the limitations of the claimed invention as detailed above except for the circuit layer comprising a passive device such as resistor, capacitor, inductor, etc.,

Saia while related to a similar method of fabricating a chip package teaches (see specifically figures 1-12) passive devices, including resistor, capacitor, inductor, etc., can be fabricated on both surfaces of the dielectric formed on the die (See Abstract).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to the proposed chip package of "Eic-148" and Kim in order to have passive devices being fabricated on the dielectric formed on the die and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

The selection of other passive devices (e.g., a waveguide in claims 284 and 335-346; a micro electronic mechanical element in claims 285 and 347-358; and a filter in claims 286 and 359-370) to be formed on the chip package would have been obvious for similar reasons set forth above.

5. Claim 317 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Eic-148" of record and Wojnarowski (5,576,517 of record) as applied to claim 282 and further in view of Saia (5,874,770 of record).

Regarding claim 317, the proposed method of "Eic-148" and Wojnarowski discloses all the limitations of the claimed invention as detailed above except for the circuit layer comprising a passive device.

Saia while related to a similar method of fabricating a chip package teaches (see specifically figures 1-12) passive devices, including resistor, capacitor, inductor, etc., can be fabricated on both surfaces of the dielectric formed on the die (See Abstract).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Saia method to the proposed chip package of "Eic-148" and Wojnarowski in order to have passive devices being fabricated on the dielectric formed on the die and such application is held to be within the ordinary designing ability expected of a person skilled in the art.

6. Claim 319 is rejected under 35 U.S.C. 103(a) as being unpatentable over "Eic-148" of record and Wojnarowski (5,576,517 of record) as applied to claim 282 and further in view of Kim (6,025,995 of record).

Regarding claim 319, the proposed method of "Eic-148" and Wojnarowski discloses all the limitations of the claimed invention as detailed above except for specifying the bump (110) being a gold bump.

Gold, however, is a known material and commonly used in semiconductor art for forming bumps as disclosed by Kim (Col. 6, lines 59+). It would have been obvious to a

person of ordinary skill in the art at the time the invention was made to select gold for forming bumps in the proposed chip package of "Eic-148" and Wojnarowski since gold bumps is commonly used in semiconductor art, as disclosed by Kim. And motivation to do so would have improved the electrical connection and prevented the oxidization of the bumps.

Conclusion

7. Applicant's arguments with respect to claims **281-370** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the newly added limitations (e.g., the underlined portions) into claims 281-370 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Luan/

Luan Thai
Primary Examiner
Art Unit 2891
November 21, 2007